# Multiprocessor DSP for Real-time Data Processing on Earth Orbiting Scatterometers

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*Abstract*--- The implementation of a Multi DSP radar signal processor for a Ku-Band Earth orbiting scatterometer is discussed. Historically, radar signal processing on scatterometers has been implemented with discrete components, FPGA's and ASIC's. These methods are expensive due to long development times, expensive tools, and their lack of flexibility. The system presented in this paper uses a radiation tolerant, space quality version of a commercial general purpose DSP (ADSP-21020) to perform the radar signal processing functions. This approach has many benefits; some of these are the ability to take advantage of development tools such as compilers, libraries, evaluation boards and emulators.

The presented system uses multiple processors interconnected with IEEE-1355 high-speed links to provide the computational power necessary. Operating systems such as Virtuoso provide core capabilities to facilitate scalability, which is important to accommodate changes in functional or performance requirements that inevitably occur late in the development cycle, or even on orbit.

A testbed has been assembled using a combination of commercial DSP hardware and spaceflight components to evaluate the proposed multiprocessing approaches. Test results of real-time radar echo processing are presented, as well as proposed designs for future investigation

TABLE OF CONTENTS

1. INTRODUCTION
2. DSP VS. EMBEDDED PROC.
3. MULTI-DSP
4. ADSP 21020
5. ASTRIUM MCM DSP
6. SCATTEROMETER
7. FAULT TOLERANCE
8. SUMMARY

## 1. INTRODUCTION

The requirement to squeeze as much science out of satellite instruments has led to various solutions and compromises to overcome downlink bandwidth bottlenecks. Weight restriction leads to the sacrifice of science due to the constraint on the amount of on-orbit processing hardware that can be flown. The solution to heavy processing requirements has been to downlink raw data for ground analysis. The ideal situation is to have unlimited downlink bandwidth and infinite on-orbit processing (MFLOPS) power. Of course the hardware available dictates otherwise.

The JPL/NASA Seawinds scatterometer launched last year measures world wide near surface ocean wind vectors on a daily basis over 90% of the ice free oceans. It performs this by transmitting a modulated chirp at 13.4GHz and measuring the backscatter cross section $\sigma_0$. The Seawinds instrument has an 803 km circular orbit and uses a rotating 0.85 meter offset paraboloid antenna to produce a pair of conically scanned pencil beams (inner and outer) at nominal angles of 40 and 46 degrees from nadir. The beams illuminate an elliptical footprint on the sea surface of about 25km wide by 50km. Return echoes will arrive approximately every 5mS. With an adjustable receive gate the number of data points can vary, requiring some elasticity built into the processing scheme.

Choosing the most powerful on-orbit processor to do the job has been limited to what is available in rad-tolerant devices. ASIC's and FPGA's fill the gap where DSP IC's are not available. Seawinds performed its signal processing using FPGA's and specialized chips for FFT handling. No space qualified processor of the DSP variety, suitable for strictly hard core number crunching has been available, until now. A Scatterometer is being developed with the aid of a testbed utilizing a prototype rad-tolerant DSP hybrid on a evaluation board.

For years the data processing load in flight subsystems projects has always been a significant factor in processor choice. The processors on a Command and Data Handling CD&H for instance must perform many tasks which can limit science processing and thus instrument performance. The embedded processor has been the answer to specific task oriented processing such as controlling modes of an instrument or routing data, whereas the DSP has been the solution to number intensive data manipulation required in such task as frequency domain analysis, filtering, image compression etc. The proliferation of DSP's in the commercial and military world attest to its value. But the lack of a suitable rad-tolerant space qualified DSP chip has

[1] 0-7803-6599-2/01/$10.00 © 2001 IEEE

been a limitation preventing the same usage in space applications. The introduction of the TEMIC TSC21020F Rad-tolerant die will change this. The added benefit of being able to utilize a number of these processor chips in parallel will allow even faster computation of algorithms and higher input data rates. This can be a significant advance in on-orbit data processing capacity.

To help organize tasks distribution operating systems exist for multi-processing systems that assist in efficiently dividing tasks among processors as well as handling complicated I/O. Operating systems are especially valuable in developing software for a large number node system where task and resource distribution can become complicated fast. Interprocessor communication becomes much more manageable when handled by the OS. We have identified a potential candidate OS should our future needs require it. Virtuoso from Eonic Systems for the 21020 processor is such an OS.

## 2. DSP vs. EMBEDDED PROC.

Embedded processors on satellites are used to control instruments, monitor engineering telemetry, controlling operational modes, repackaging and distributing science and telemetry data, and also for limited scientific processing. Traditional processors have had limited to no data analysis duties. The introduction of the digital signal processor with its unique architecture came about due to the need to gather data real time and process it, a very computationally intensive effort. The architecture of a DSP chip is designed to handle certain algorithms such as FFTS as quickly as possible. The processing performance of flight processor has always been less than that of the equivalent commercial version due to the radiation tolerancing. Yet space qualified MIPS has evolved over time from the days of Voyager to today's new scatterometers and instruments. Table 1 illustrates the growth in standard processors.

**Table 1** Processor Performance Evolution

| SPACECRAFT | MIPS | YEAR |
|---|---|---|
| Voyager | 0.003 | 1977 |
| Galileo | 0.6 | 1989 |
| Cassini | 1.2 | 1997 |
| Mars Pathfinder | 17.5 | 1996 |
| Seawinds on QuikScat | 21.2 | 1999 |

These numbers are given in MIPS which are not the same as MFLOPS. The TSC21010F, for instance, is capable of 40 MFLOPs. A DSP processor is optimized for certain algorithms which are not considered when stating MIPS numbers on a standard processor. The same algorithm run on a standard processor can take orders of magnitude longer to run even if its MIPS are higher than the DSP with its MFLOPS. An accurate comparison requires a common benchmark standard executing on both processors. Such characterization is part science part art. Generalized comparisons have shown a 20 MFLOPS DSP processor is equivalent to a 120 MIPS RISC processor when running an FFT. Although the computational power of standard processors has been increasing they still cannot handle the raw real time data processing that is required of a typical mission, thus specialized hardware implementations are the obvious solution.

The scatterometer require still more power than one processor (50 MFLOPS) alone can deliver. By paralleling DSP chips (20 MFLOPS) their effective power is significantly magnified. In the past DSP has been used on flight projects but usually in an FPGA or ASIC design which incur heavy development costs, and have very limited scaling potential. ASICS and FPGA also do not lend themselves to late design changes or more importantly on-orbit reprogramming. The use of commercial Multi-Dsp allows for a milestone in science processing capability on flight projects.

*Why DSP is better*

- Many MFLOPS dedicated to a single task
- Scalable to multiple processors
- Faster I/O(Real Time)
- Compact and deterministic code(Exec. time)
- Limited Latency
- Low Power
- Zero Overhead Loops

When choosing a processing method for science data on orbit other factors than MIPS/MFLOPS warrant some consideration. These include power budgets, weight issues, life cycle and cost. Initial evaluations show the DSP processor to have an overall advantage. Its power requirements at 100% load are more than an equivalent FPGA but not significantly. The cost of the Rad-tolerant 21020 is much less then a similar FPGA. General Purpose DSP processor technology is a powerful processing tool that can be reconfigured quickly for different jobs.

## 3. MULTI-DSP

The power of a single DSP chip can be magnified by the use of multiple chips running in a parallel or simultaneous mode. By taking an algorithm or task and dividing it among several processors it can be performed much quicker than a single processor alone or the input data stream can be time sliced, with slices of data being routed to multiple processors running identical algorithms. The ideal leveraging occurs if each processor contributes one hundred percent to the overall task working at the same time as the other processors and none are idle. Equation (1) illustrates ideal leveraging.

$$MFLOPS_{SYSTEM} = p * MFLOPS_{SINGLE} \quad (1)$$

p is the number of processors in the system. But there is no free lunch, the use of multiple processors introduces a new set of issues in the development plan. First is the associated overhead in coding necessary to manage communication among the processor nodes. Secondly the interconnect scheme necessary to share the data also requires intelligent design and is dependent on the task to be run. Determinations are based on the algorithm dependencies being processed and timing requirements. A multiprocessor system can be inter-connected in various schemes, each having unique overhead burdens, the scatterometer will attempt to use the simplest interconnect topology capable of performing the task as well as giving flexibility and fault tolerance.

The advantages of a multiprocessor system is having each node executing a task in parallel with other nodes. The task can be different programs operating on real time input data or the same program operating on real time input data. The two common methods of distributing workloads are SIMD and MIMD[1].

Single Instruction Multiple Data (SIMD), takes varying input data and runs the same code on each node. Everything being controlled by a master DSP processor. A common memory is shared among all the processors.

Multiple Instruction Multiple Data (MIMD), takes varying input data and also breaks up the algorithm spreading it among the various nodes. Memory can be globally shared by all the nodes or locally only available to one processor. Any task must be capable of being broken up into subtasks if it is to be processed by a multi-dsp system. Excessive idle time is inefficient, and contention to resources in various forms leads to waste of processor time. Resource conflicts can be; access to memory, I/O waits, or access to a bus. The present scatterometer design requires no data sharing among processors except to send output results to the TX DSP, thus eliminating shared buses, memory and any associated conflicts. Main concerns of the scatterometer will be about synchronization of data and fault tolerance schemes.

## 4. ADSP 21020

The TSC 21020 from Temic is a 32/40 bit DSP capable of 30 MFLOPS at 15MHz EDAC memory protection enabled (faster without). It is based on the Analog Devices ADSP-21020 which has an existing history with extensive experience existing on its use in various commercial applications. A true and tried development kit exist that aid in all aspects of writing , debugging and testing of software that will execute on the 21020. The tools included in this are the Compiler, Assembler, Simulator, Debugger, and Libraries, and incircuit emulator (EZ-ICE) exist for loading and debugging code. The EZ-ICE utilizes the JTAG port on the 21020 for its access, a well known standard. The Rad Hard TSC21020F total dose capability is specified as 100 krad(Si). It's latchup immune, and the SEU threshold is stated to be >50 MeV/mg/cm^2.

## 5. ASTRIUM MCM DSP

The Astrium Multi Chip Module (MCM) DSP is a radiation tolerant hybrid that incorporates the TSC21020F processor as well as allows various peripherals to be connected to it via the Peripheral Interface IC which make a possible contender for a turnkey DSP system requiring limited hardware and software design man hours. Fig. 1 shows the layout of the eval board containing the hybrid chip. Some of the hybrid features are;

- Peripheral Controller ASIC
- IEEE 1355(SpaceWire) High Speed 150Mbit/s serial links
- JTAG
- User Interface UART, FIFO, I/Oport
- 50krads(Si)
- Latch Up immunity better than 100Mev
- SEU LET threshold better than 15 Mev/cm/mg
- 6 watts at 100% load
- 128K Data Memory
- 128K Program Memory

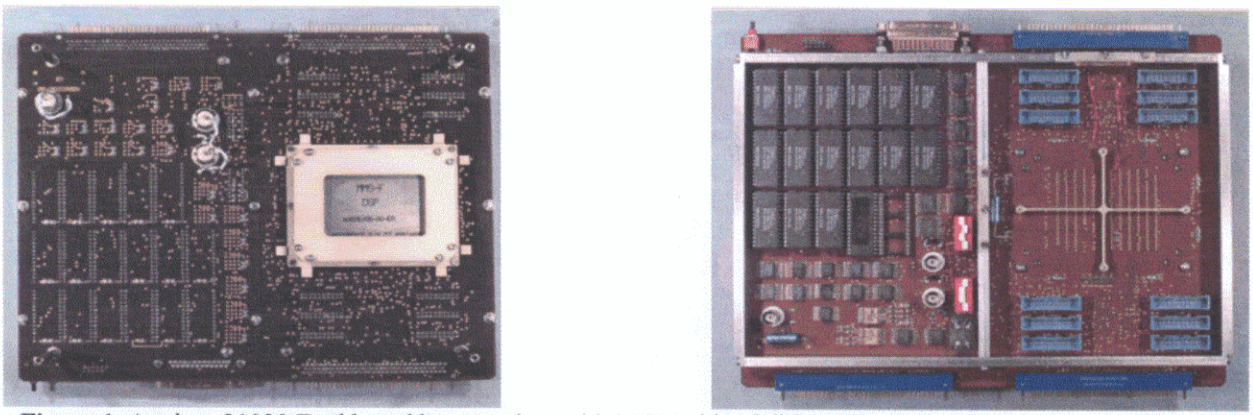

**Figure 1** Astrium 21020 Eval board bottom view with MCM chip visible and top view with memory and ports visible

These are being used to assemble our breadboard scatterometer

## 6. SCATTEROMETER

The scatterometer being bread boarded has the luxury of being tested on a flexible testbed assembled for the purpose of trying different hardware configurations and testing software algorithms. By bringing together various pieces of hardware, development tools and subsystems we can test at the individual component level as well as at the end-to-end level; recording performance, benchmarking and evaluating as we define our requirements

the main CD&H processor for science data transfer. It also performs basic error checking to verify the receive processors are operational. The receive processors perform the real time data processing and forward it to the transmit processor for relay to the CD&H. Data transfers happen over the SpaceWire link. Eliminating a shared bus eliminates much if not all hardware contention. Synchronization is accomplished by operating all processors from a common clock source. Synchronization allows knowledge as to which receive echo pulse is being processed by which node. This is accomplished by the transmitter node and a dedicated hardware synch. line. If the PRF should increase or other loads are introduced that can lengthen the amount of time a processor has to finish

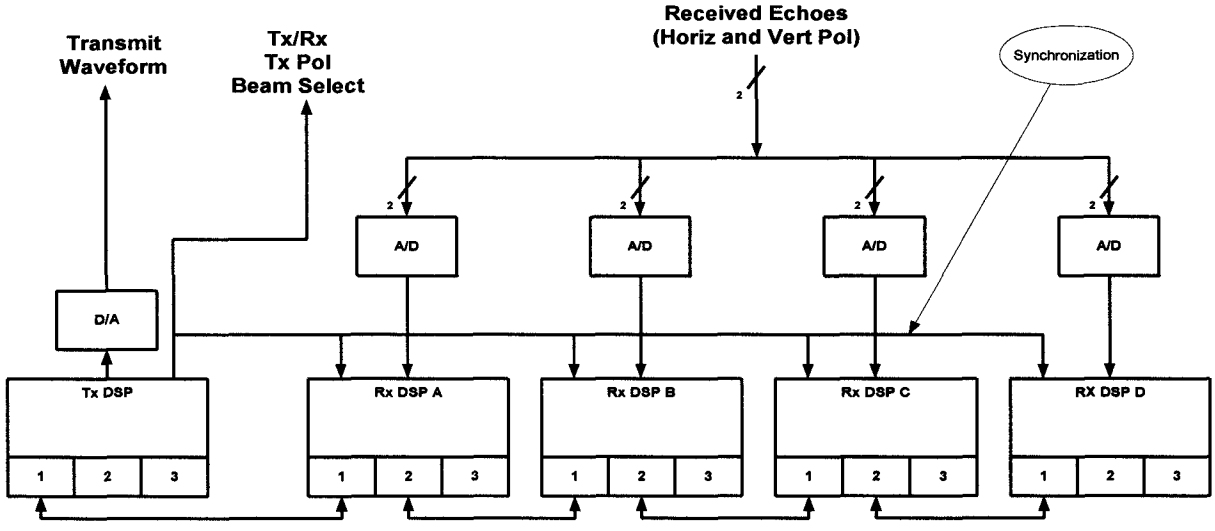


**Figure 2** Block diagram showing DSP processor connection scheme

An initial scatterometer design has been proposed that transmits a modulated chirp, receives a return echo of horizontal and vertical polarization's, downconverts, digitizes, then sends the inputs to a DSP receive chain for processing. Fig. 2 is a block diagram showing the various processors, the A/D's, SpaceWire connections and a synchronization line. This scheme is implemented using several DSP processors performing either the Tx or the Rx function. The processors are connected in a round robin fashion to allow message passing among them via the SpaceWire link and to support fault tolerance. The transmit processor performs the transmit function and directs the operation of the several receive DSP's, each of which acquires and processes a single echo of the input data stream.

This multiprocessor topology is different than most other multiprocessor system in that each node has it's own memory as well as processing its own code. We have implemented a multiprocessor system where each task (echo) has its own processor, in contrast to the classical multiprocessing paradigm of a single task divided among multiple processors. The transmit processor, besides generating the transmit data and controlling which node processes received return data, also communicates with a job other processors (nodes) can be added with relative ease, this will be designed for a worst-case processing requirement and a fixed number of processors will be used.

The scatterometer breadboard uses three Astrium evaluation boards connected via the SpaceWire serial link and a SpaceWire simulator running on a PC that duplicates additional nodes, although no processing of data can be done on the simulator.

Initial end-to-end tests takes simulated radar returns generated by a model and signal generator and inputs them to the scatterometer processors. The results are then evaluated for accuracy. This is performed in real time for a number of PRF's. The system will be monitored for timing errors, glitches, data skips, jitter, latency and worst case scenarios. The breadboard

is flexible enough to allow evaluation of various fault tolerant strategies, for example what happens if we lose a receive processor.

*One complete cycle*

The cycle begins with the transmission of a modulated chirp and the transmit processor readying a receiver processor for the echo. The returns are sent to a predetermined free receive processor by the transmit processor. Worm hole routing allows for messages and data to pass through each processor without any delay along the SpaceWire link. This is required to send status and data to the transmit processor as well as commanding from the tx to the rx processors. We operate in a standard Multiple Instruction Multiple Data (MIMD) mode because the algorithms operate independently but employ elements of SIMD due to the fact that the Tx processor synchronizes parsing of return echoes[2]. The transmit node sends the return echo to a predetermined idle receive processor where the echo is dechirped, filtered, decimated, FFTed and binned. The processed data is sent back to the transmit node where it is then forwarded to the main CD&H processor a VME based RAD6000 for packetizing and downlinking. This system allows scaling up by adding in idle processors easily, they would be already attached in parallel to the input data stream being idle or operating at reduced load, for fault tolerance purposes or heavier computation requirements. SpaceWire links must be attached to the nearest neighbor to complete the round robin configuration. We can test the receive processors by performing an end to end test, loading know data into the input of our receive chain and verifying outputs. This gives us a quantitative checkout of receivers.

Initial efforts have been to procure all the necessary hardware and then begin writing driver software for the SpaceWire links. The code will be written in the 21020 assembly language. Filter and FFT algorithms are selected and tested for performance. Execution speed and bandwidth parameters will be evaluated. A complete end –to-end system with multiple processors is then assembled and tested for various timing characteristics as well as data integrity. Fig. 4 shows the lab setup with three Astrium eval boards in test fixtures, a PC running the Incircuit emulator , and the SpaceWire cabling.

Although we initially considered utilizing the Virtuoso operating system, it turns out that our DSP effort is simple enough to attempt all coding and driver creation ourselves. The learning curve for Virtuoso is not justifiable at this point but certainly remains an option should this project become more complicated or for future space DSP projects.

## 7. FAULT TOLERANCE

Whenever a system becomes more complicated, has more parts, more switching, etc. more opportunity exists to suffer a fault, error or some sort of degradation of performance. Although a multiprocessor system is inherently more complex it also lends itself to unique fault protection through smart design and implementation. By utilizing non-faulted processors to carry the processing of the failed processor an operational system is still on-orbit. The success of this depends on designing margin and not utilizing 100% of the system 100% of the time. By having extra processors as well as a reliable switching method a dynamically reconfigurable instrument is possible minimizing any single point failures. Data can also be processed on a spare or idle node for error comparison. Tests or calibration signals with known characteristics can be loaded on-orbit outputs examined for errors to assist troubleshooting.

With the existence of a Rad-tolerant MCM the space environment can be made accessible to DSP. By designing for efficiency, and redundancy a robust data analysis package can be flown.

## 8. SUMMARY

The availability of a Rad-tolerant General Purpose DSP processor hybrid allows the rapid development of a scatterometer that is very flexible and due to multi-processing capabilities very powerful. The scatterometer testbed will show the ability to connect several processors together via the SpaceWire link and process simulated radar echoes in real time. Should more algorithm processing power be required it is trivial to add more processors to the hardware and accommodate new scenarios. The ability to fly a multiprocessing system opens new opportunities for science processing on orbit such as data compression, spectrum analysis, and image processing. Fault tolerance, error correction and reliability issues can be accommodated to the degree desired. The evolution of a commercial DSP processor to flight has enormous potential, especially for low cost quick turn around projects.

## ACKNOWLEDGEMENTS

The work performed in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Much much thanks goes out to the individuals who contributed many hours coding in 21010 assembly working to our milestones.
Kouji Nishimoto, Minh Lang, Ben Wilkinson.

This work would not have been possible had not ASTRIUM, specifically Pierre-Eric Berthet, given us an

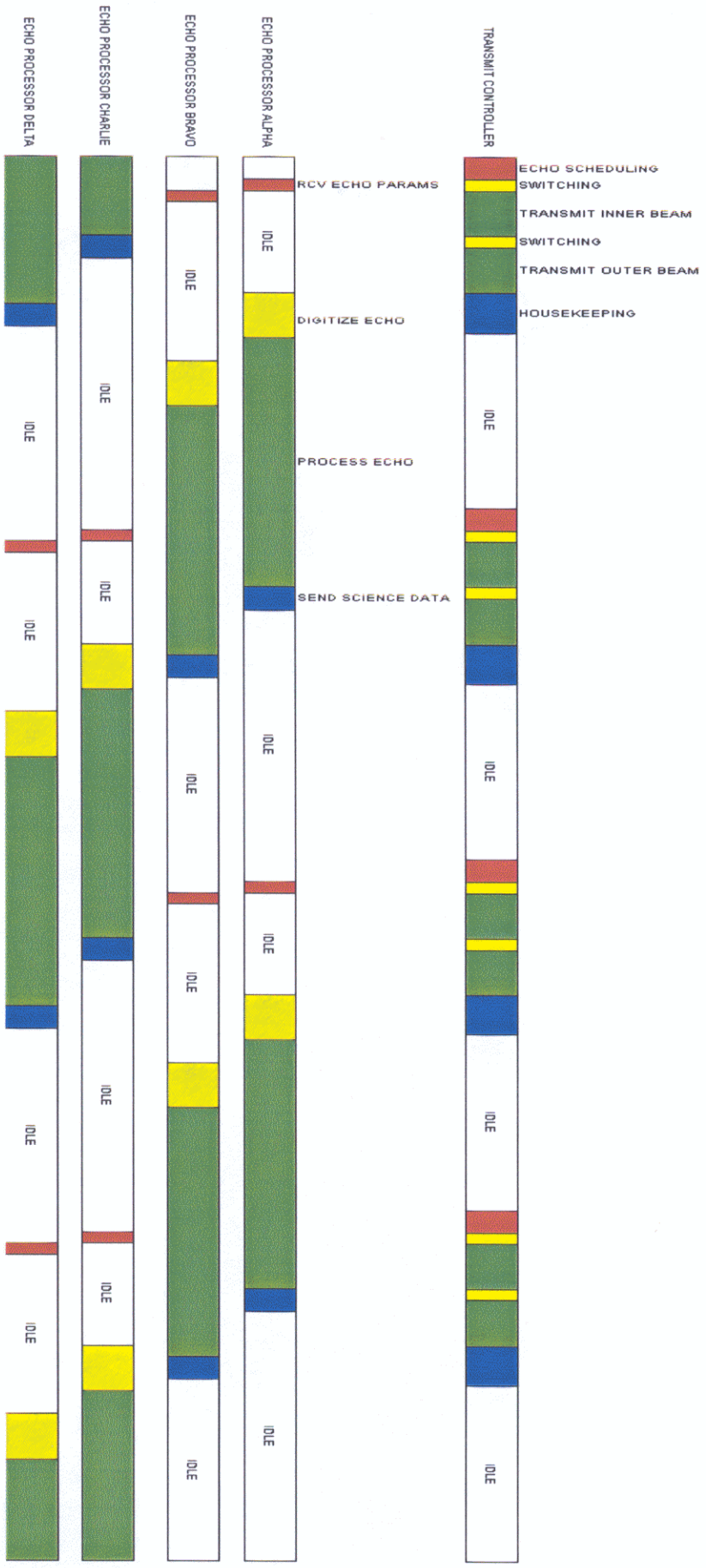


**Figure 3** Scatterometer Processor Timing

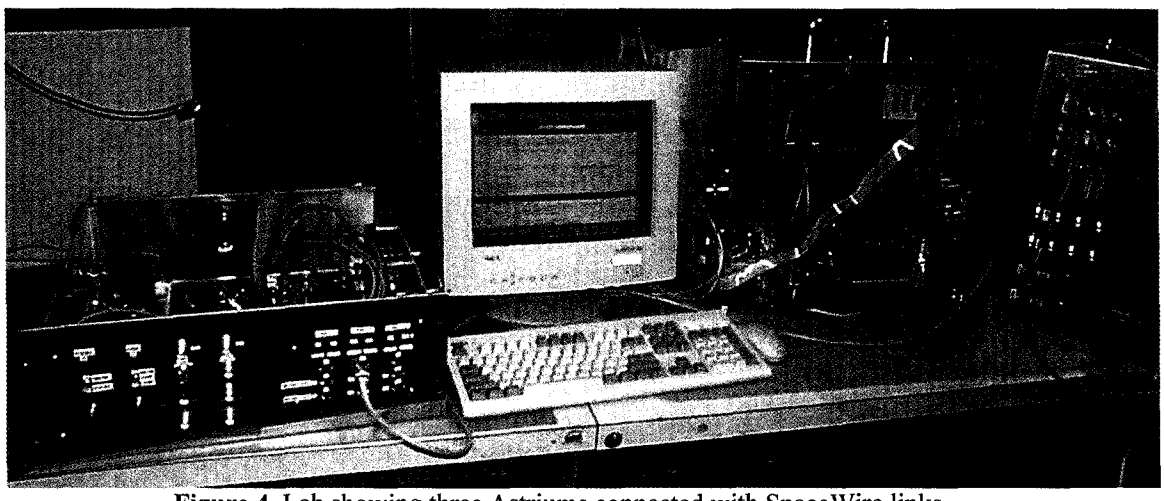

**Figure 4** Lab showing three Astriums connected with SpaceWire links

extended loan of the MCM DSP hybrids on the eval boards.

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[2] A. ZOMAYA, *Parallel & Distributed Computing Handbook*, New York, NY: McGraw-Hill 1996.

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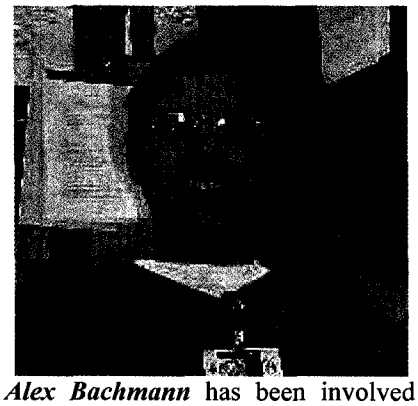
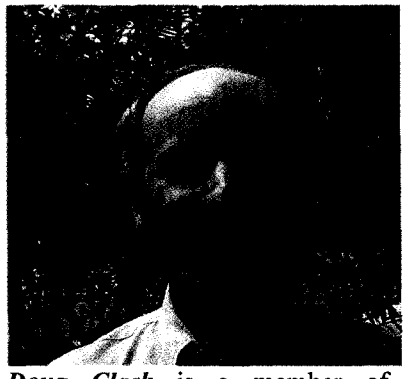
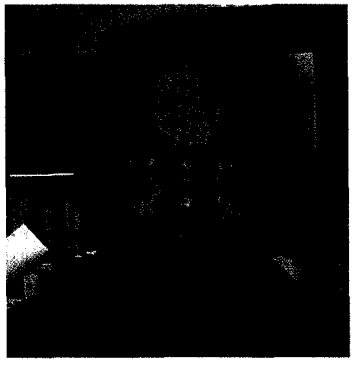


***Alex Bachmann*** has been involved in Spacecraft and Ground System Test and Integration for 15 years. His interests at JPL include developing test methodologies for command and data handling systems as well as advancing DSP technology on space projects.



***Doug Clark*** is a member of the Flight System Engineering Group within JPL's Avionics System Engineering Section. He earned a Bachelor's degree in Physics from San Diego State University and a Master's degree in Physics from California State University, Los Angeles. At JPL he has been involved in the test and integration of command and data handling systems for scatterometers, and is currently developing system architectures for future instruments.

***James Lux*** is in the Spacecraft Telecommunications Section at JPL. Scatterometers design is only one of Jim's diverse interests, which range from man-made tornadoes to solar eclipses to high performance digital radio links.



***Richard Steffke*** graduated California State Polytechnic University Pomona BA Aerospace Engineering. He was lead test engineer on NSCAT DSS, which was the first scatterometer to fly a DSP.

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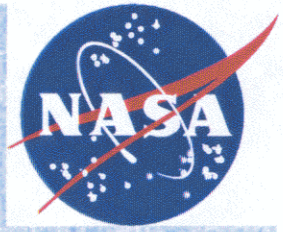


# Multiprocessor Digital Signal Processing On Earth Orbiting Scatterometers

BY

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Pasadena, CA

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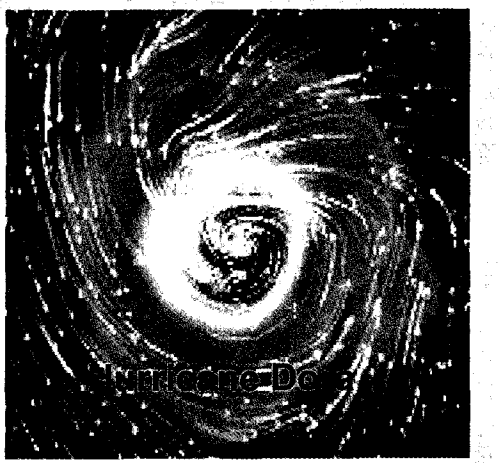
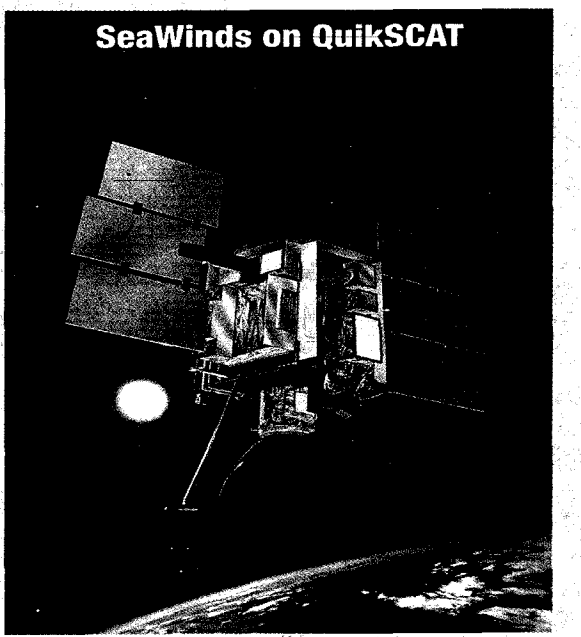
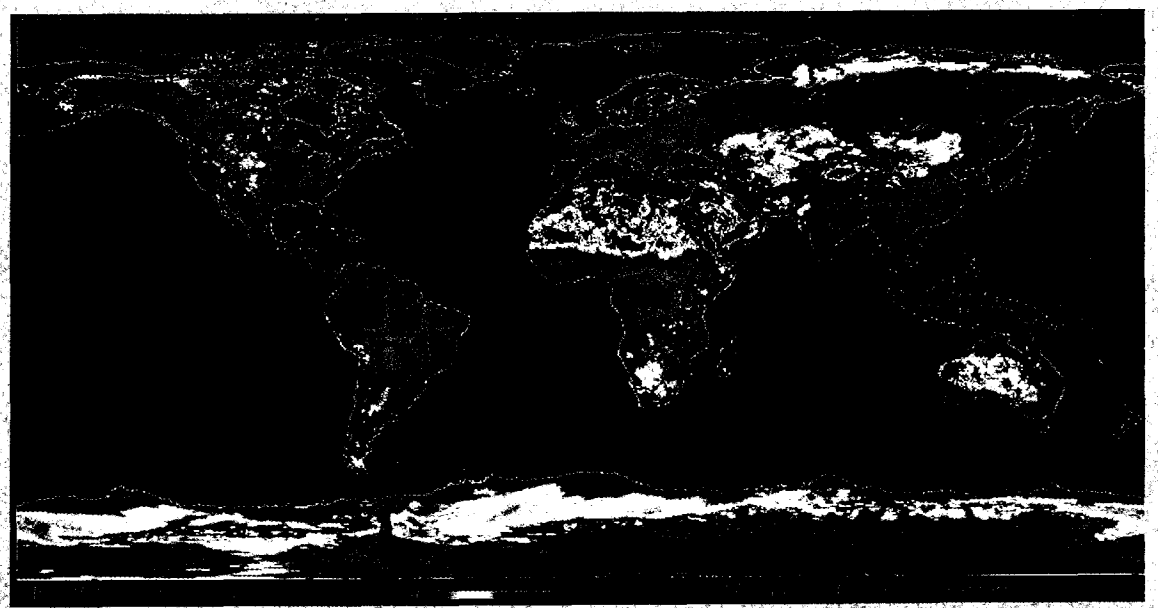
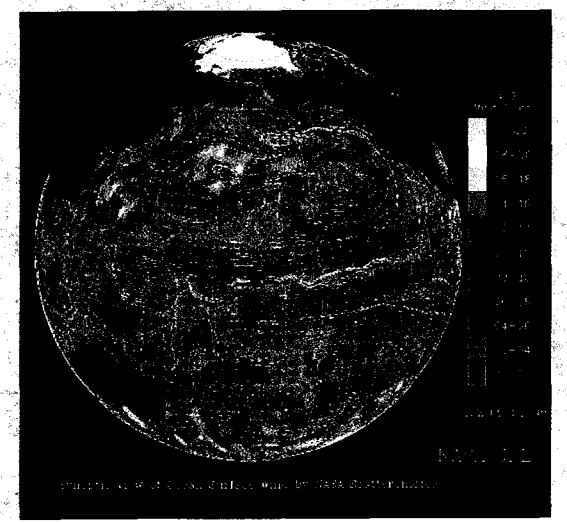
# SeaWinds Scatterometer




13.402 GHz
1.5 ms Pulses
375 kHz chirp
110 Watts
803 km orbit





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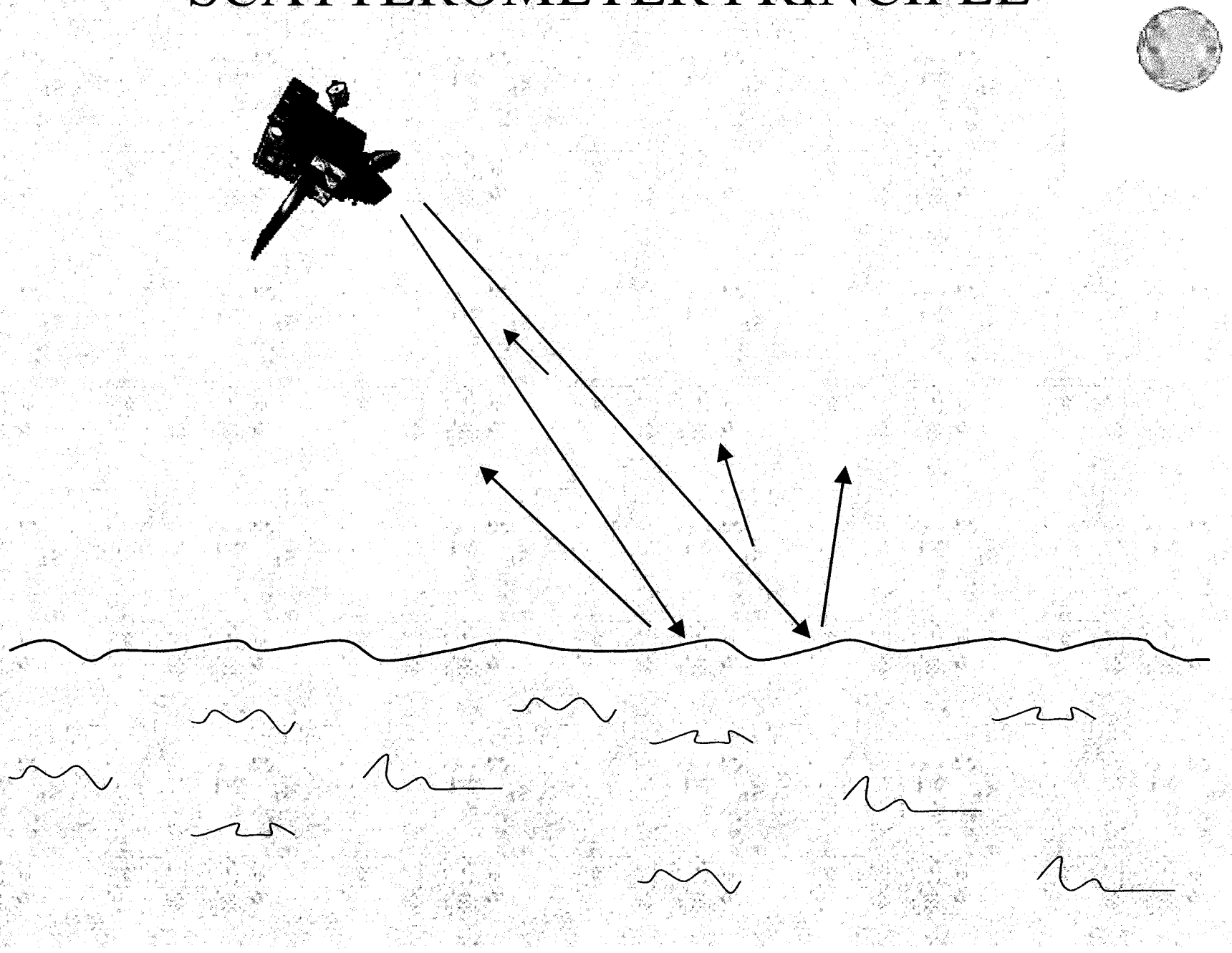
# SCATTEROMETER PRINCIPLE



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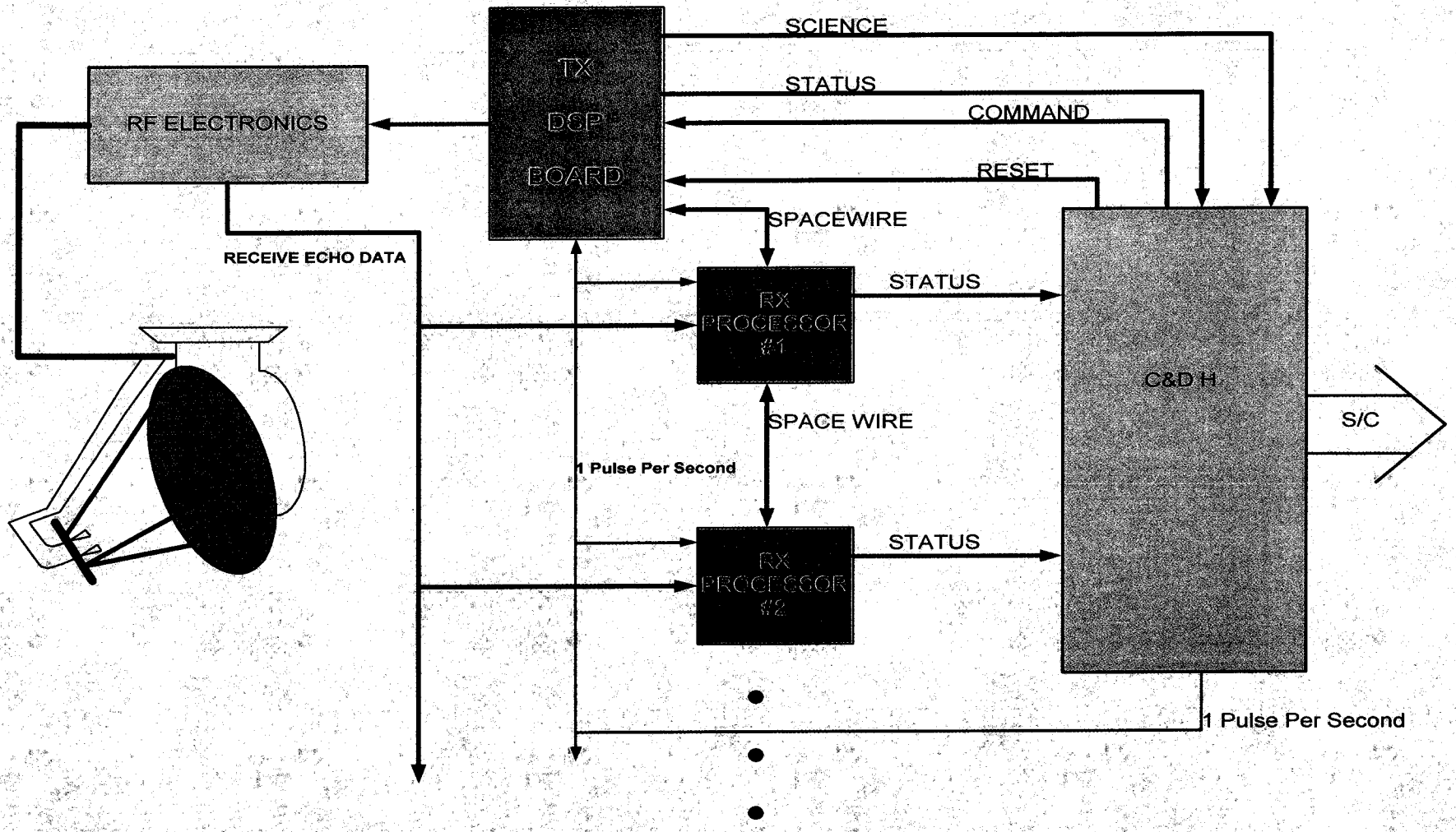
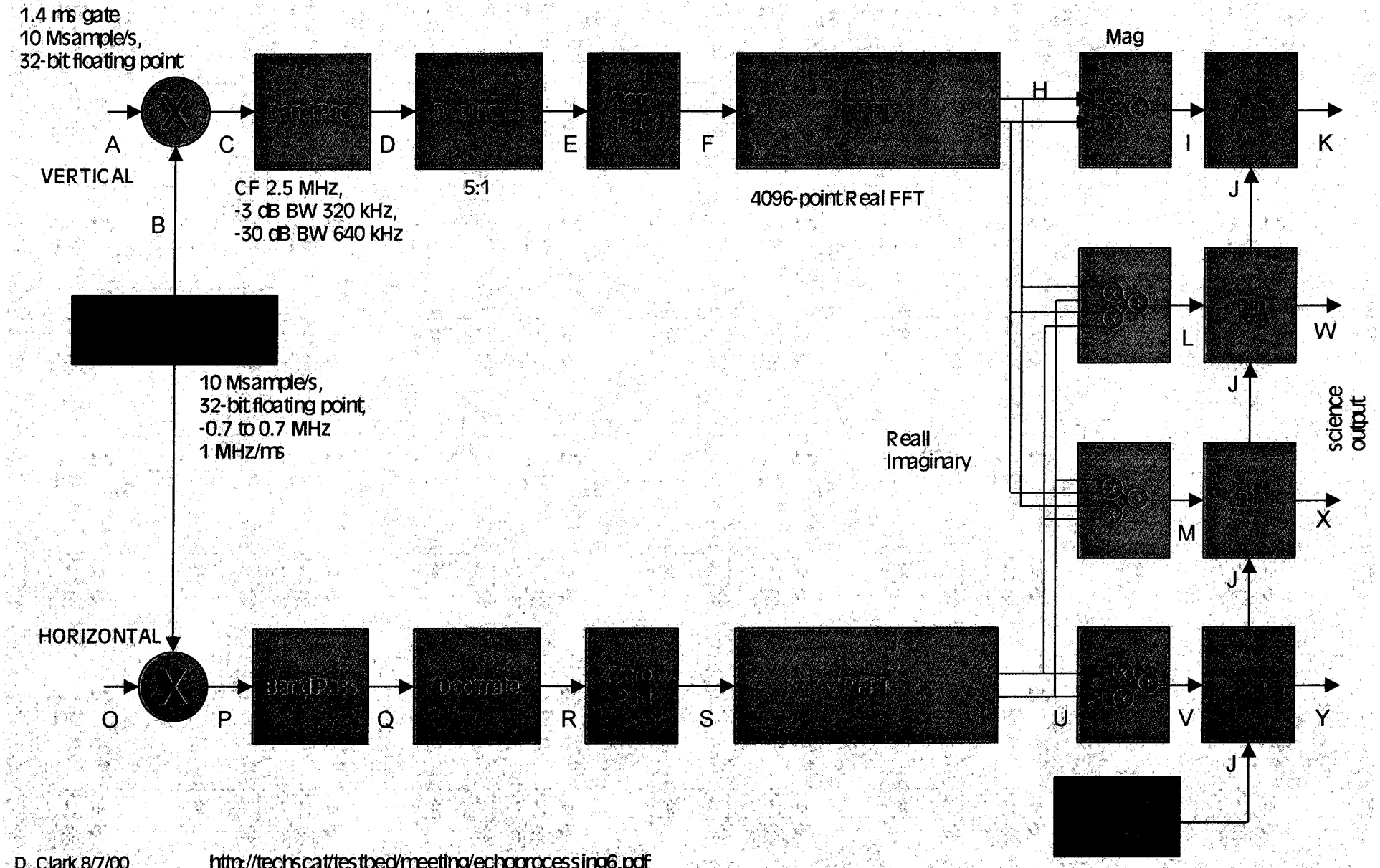
# RADAR SYSTEM BLOCK DIAGRAM



# Baseline Echo Processing Parameters



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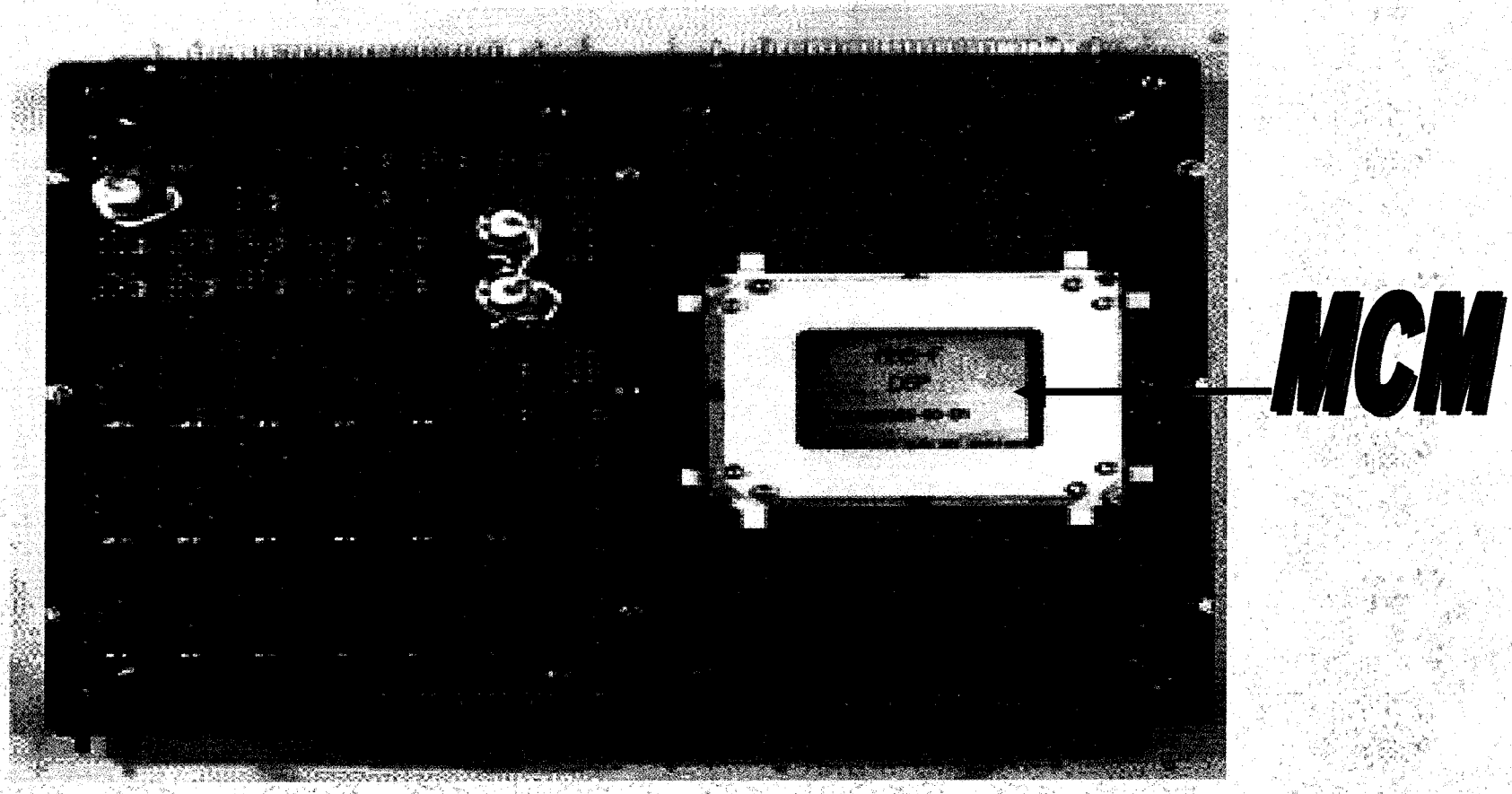
# EVAL BOARD WITH MULTI CHIP MODULE



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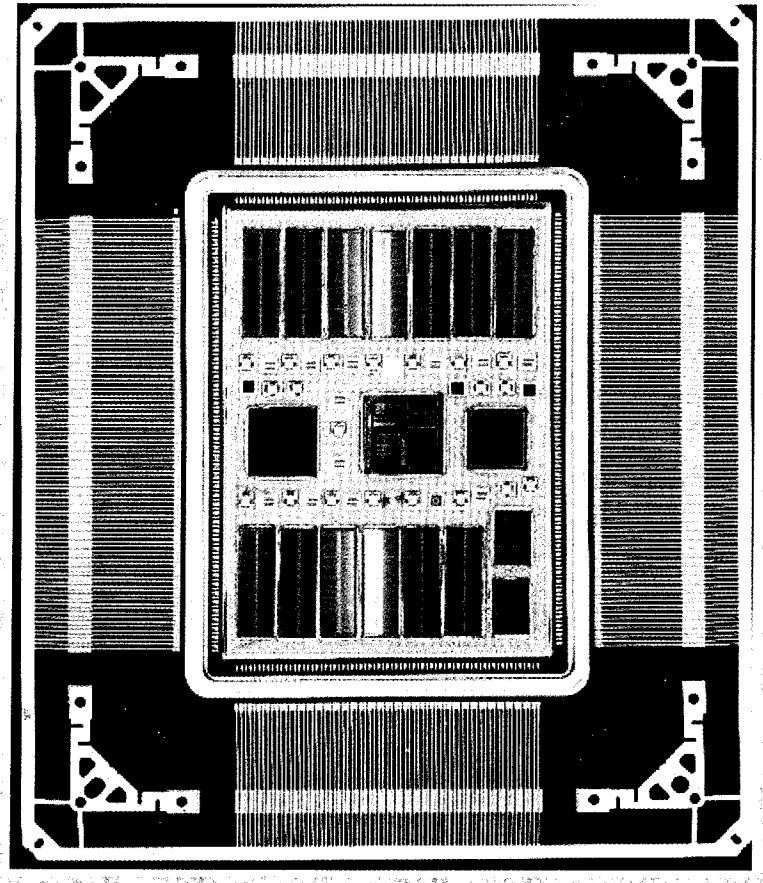
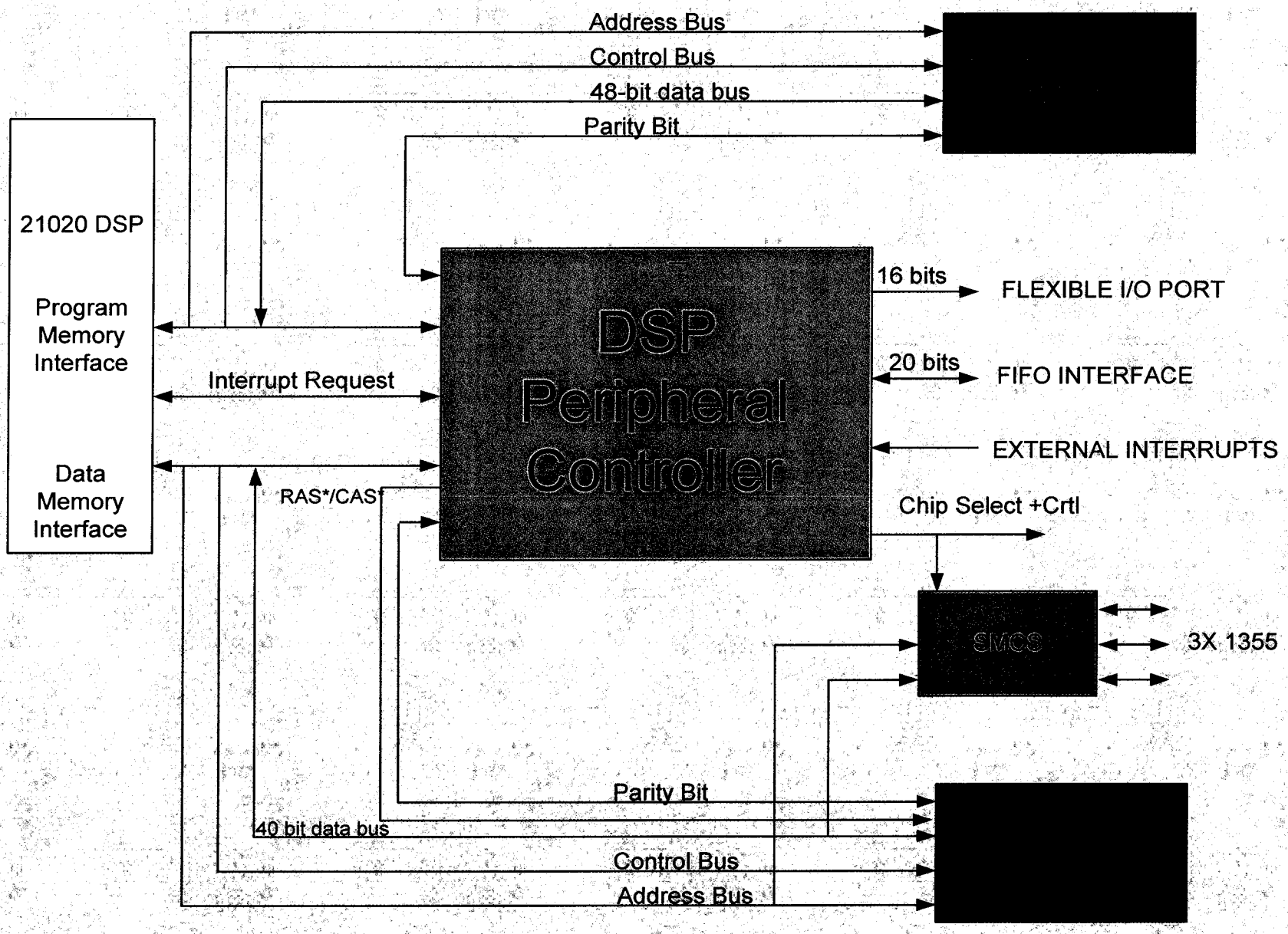
# ASTRIUM MULTI CHIP MODULE

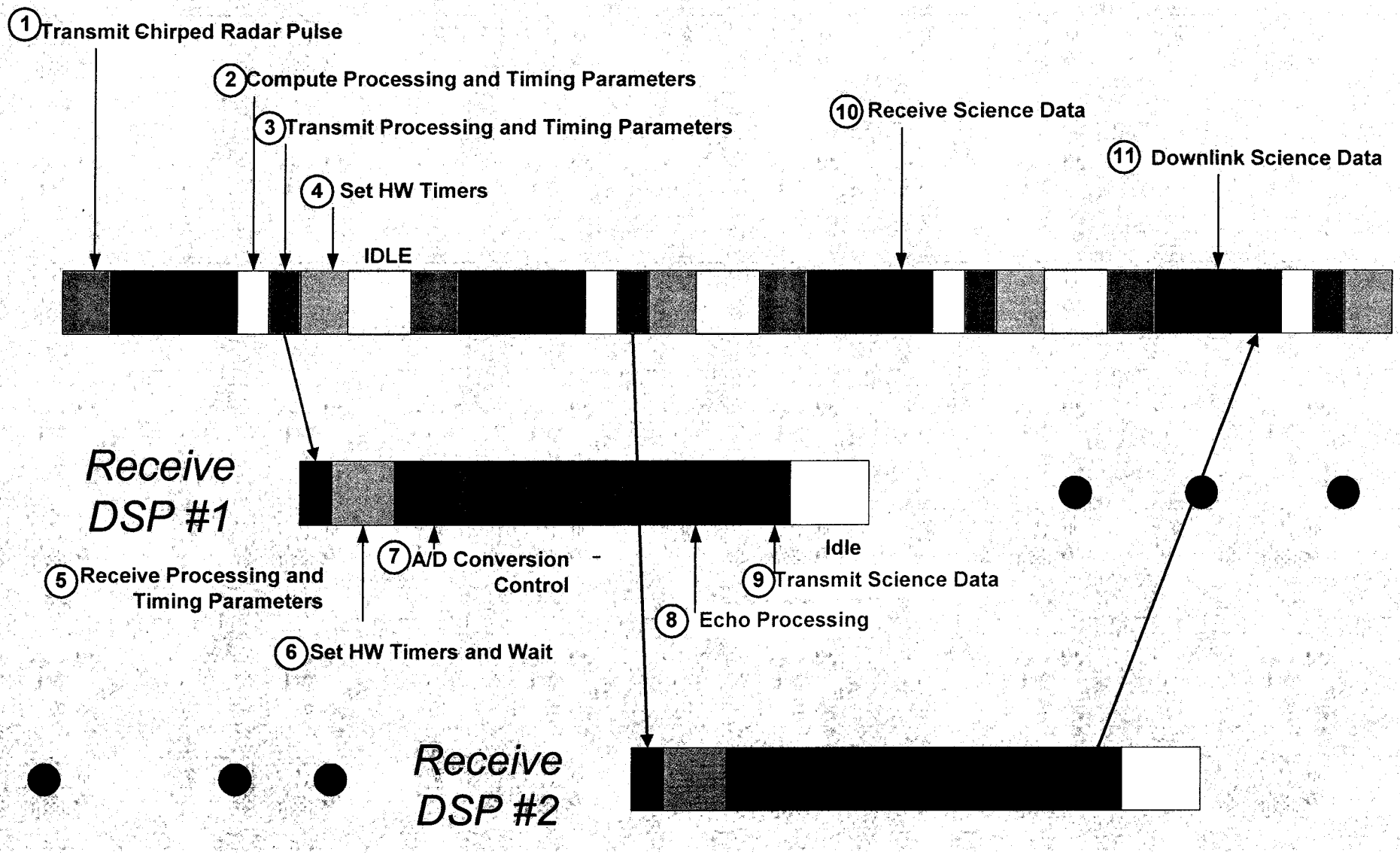


- TSC21020E DSP fabricated by Temic,
- 2 x 8k x 16 Dual Port RAM
- 15 MHz / 30 MFLOPS (0 WS) when EDAC protection is enable
- 128kwords EDAC protected SRAM for the Program emory
- 128kwords EDAC protected SRAM for Data Memory,
- 3 x 1355 interfaces
- 256 x 20-bit FIFO interface
- 16-bit versatile IO port (Serial In/Out interface, Parallel In/Out Interface, UART, Pulse Generator)
- JTAG interface for test ( Boundary Scan test includes TSC21020, DPC and SMCS)
- Temperature range : -55 to +125 °C
- Power consumption : 6 W typical
- Reliability better than 100 FITs
- Radiation Tolerant better than 50 Krad,
- Latch Up immunity better than 100 MeV
- SEU LET better than 15 MEV/cm2/mg

# MCM BLOCK DIAGRAM



# Transmit and Receive Timing



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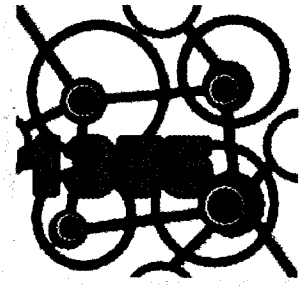

# 1355 SPACE WIRE

- 1355 is asynchronous, auto baud, point-to-point, and very simple.
- 1Mbp/s up to 200 Mbp/s, and protocol compatible versions are being developed up to 2Gbp/s.
- Rad-Hard Devices available
- The minimalist packet protocol of 1355 makes it particularly easy to embed other protocols within it. So, for example, the same network can be carrying ATM and MPEG and IP and raw disk sectors and even memory accesses, and all with negligible additional protocol overhead.
- http://www.estec.esa.nl/tech/spacewire/

JPL

# CONCLUSION

- FUTURE GOALS
  - End-to-End Prototype Radar
  - Optimize Code and Algorithms

**RESULTS**

- DSP IS POWERFUL
- DSP IS FLEXIBLE
- DSP IS COST EFFECTIVE(Many programmers available)
  - Quick Development
  - Low Cost Parts (~$30k per Rad Hard MCM)
- DSP ALLOWS FLEXIBLE FAULT TOLERANT DESIGN
- DSP IS PROLIFIC(Strong history, many applications)
  - Image Processing
  - Spectral Analysis
  - Code Compression